ABSTRACT

Please amend the abstract as follows:

An RSD FET device with a recessed channel is formed with a raised silicon [[S/D]] sources and drains and a gate electrode structure formed on an SOI structure (a Si layer formed on a substrate) by the steps as follows. Form a SiGe layer over the ~~silicon~~ Si layer and a RSD layer over the SiGe. Etch through the RSD layer and the SiGe to form a gate electrode space reaching down the ~~silicon~~ Si layer. Form a pair of RSD regions separated by the gate electrode space. Line the walls of the gate electrode space with an internal etch stop layer and an inner sidewall spacers. Form a gate electrode inside the inner sidewall spacers on the ~~silicon~~ Si layer. Form external sidewall spacers adjacent to the gate electrode between the RSD regions next to the inner sidewall spacers, and dope the RSD regions, whereby a recessed channel is formed in the SOI silicon layer between the raised source/drain regions thereabove and [[above]] below the level of the SiGe layer.